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Mentor revamps analog, mixed-signal IC design flows

By Stephan Ohr
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SAN FRANCISCO — In an effort to reposition itself against the incumbent in the analog tools world, Mentor Graphics Corp. will announce this week enhancements to its front-to-back tool set for analog IC design. Called Advance MS (ADMS), the tool set incorporates all high-level languages, advanced circuit simulators, and layout and verification tools, complete with parasitic extraction, schematic comparison and back annotation.

Mentor Graphics believes the new package will offer language support and fast simulation to new-generation system-on-chip designs incorporating analog and RF peripherals, as well as processors and memory. These designs include digital SoCs with a dominant amount of analog circuitry, as well as digital designs with a small amount of analog.

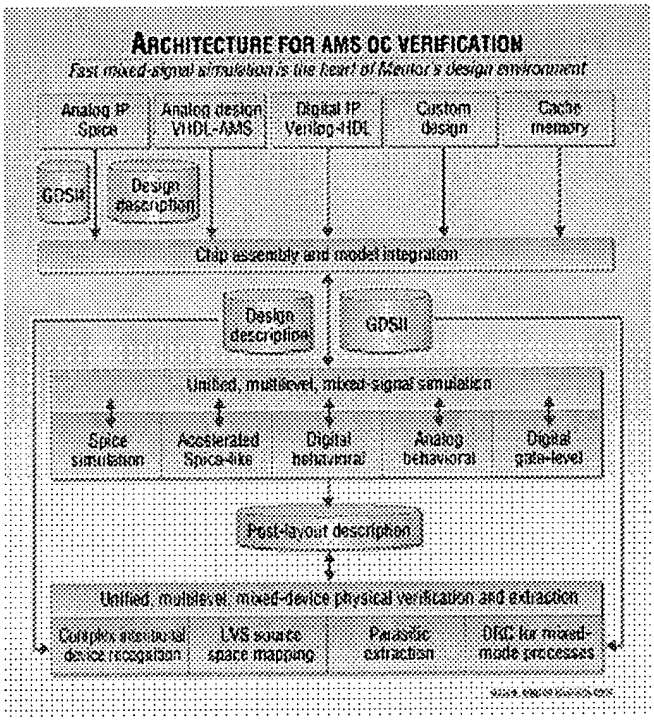
"DSP communications devices, for example, once included a little bit of analog," said Wally Rhines, Mentor's president and chief executive officer. "They are now including more and more analog on the chip."

These integrated analog blocks include analog-to-digital and digital-to-analog converters, phase-locked loops, RF modules and adaptive filters. The ADMS design flow gives SoC designers the ability to examine performance at the highest level in advance of pushing each block through its own flow. At final chip assembly, ADMS tools will complete functional verification at the full-chip level.

At the heart of the ADMS tool set is a single-kernel, language-neutral simulator that combines four high-performance simulation engines in one tool: Eldo for general-purpose,

large-signal model simulations; ModelSim for digital simulations; Mach TA for fast transistor-level simulations; and Eldo RF for modulated steady-state simulation.

The glamour item is Mach TA. Mentor's Eldo simulator, which would automatically partition circuits between MOS transistors that can be modeled with relaxation algorithms, and full-feedback circuits requiring more rigorous mathematical modeling, had always claimed to run faster than conventional Spice. Though Mach TA can also take a standard Spice netlist as its input, it is an entirely different modeler, Rhines insisted. It's 1,000x faster and still provides accuracy to within 3 percent of Spice, he said. For full-chip, transistor-level simulation, the Mach TA simulator offers users the ability to trade accuracy for speed, Rhines said.



To be sure, the Eldo RF option adds both harmonic balance and time-domain simulation to the ADMS package. Built upon the Eldo analog simulator, Eldo RF includes algorithms specifically geared toward RF ICs operating in the GHz range. Applications for the modeler include transceiver components like low-noise amplifiers, mixers and voltage-controlled oscillators. With Eldo RF integrated in the ADMS simulation environment, ADMS uses a modulated steady-state analysis algorithm to model digitally modulated RF signals.

Full-chip verification

With Calibre xRC, Mentor applies its core Calibre extraction technology to the specific requirements of analog/mixed-signal design. Traditionally, parasitic extraction has forced SoC designers to harness a small arsenal of tools. In the analog/mixed-signal IC design flow, Calibre xRC can replace this unwieldy lot with a single multipurpose tool.

The product provides parasitic extraction for a full-chip, digital

circuit extraction, and back annotation — complete with naming conventions, said Rhines. "None of the extractors go down to the transistor level," he said. "This one will do it."

The ADMS tool set provides high-level language support, including verification support for Verilog AMS. The design flow uses a single netlist hierarchy that allows designers to freely combine VHDL, Verilog, VHDL-AMS, Verilog-AMS, Spice and C anywhere in the design. This enables both top-down design and mixed-level simulation for bottom-up verification.

The tool set includes the Design Architect-IC tool (an SoC design "cockpit"), and the IC Station chip assembly solution, for physical layout, top-level floor planning and routing. It runs on Linux, HP and Sun platforms and even talks to the Cadence Analog Artist Environment.

"Deep-submicron design is where mixed-signal design becomes real. You need to integrate it and not throw it over the wall," Rhines said.

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[Abstract] [PDF Full-Text (284 KB)] **IEEE CNF**

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ASIC Conference and Exhibit, 1992., Proceedings of Fifth Annual IEEE International , 21-25 Sept. 1992
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Electrotechnical Conference, 1994. Proceedings., 7th Mediterranean , 12-14 April 1994
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Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia and South Pacific , 28-31 Jan. 1997
Page(s): 189 -194

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Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IEEE International Symposium on , Volume: 4 , 28-31 May 2000

Page(s): 721 -724 vol.4

[Abstract] [PDF Full-Text (296 KB)] **IEEE CNF**

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Matsuzawa, A.;
Quality Electronic Design, 2001 International Symposium on , 26-28 March 2001
Page(s): 97 -104

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Hoff, J.R.; Mekkaoui, A.; Christian, D.C.; Zimmerman, S.; Cancelo, G.; Kasper, P.; Yarema, R.;
Nuclear Science, IEEE Transactions on , Volume: 48 Issue: 3 , June 2001
Page(s): 485 -492

[Abstract] [PDF Full-Text (100 KB)] **IEEE JNL**

11 **Behavioural modelling of mixed-signal circuits using PWL waveforms**
Long, D.I.;
Mixed-Signal AHDL/VHDL Modelling and Synthesis (Ref. No: 1997/331), IEE Colloquium on , 19 Nov. 1997
Page(s): 2/1 -2/6

[Abstract] [PDF Full-Text (456 KB)] **IEE CNF**

12 **Guided-probe diagnosis of macro-cell-designed LSI circuits**
Kuji, N.;
Test Symposium, 1997. (ATS '97) Proceedings., Sixth Asian , 17-19 Nov. 1997
Page(s): 174 -179

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Devices, Circuits and Systems, 2000. Proceedings of the 2000 Third IEEE International Caracas Conference on , 15-17 March 2000
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Wilson, P.R.; Chapman, P.; Ross, J.N.; Brown, A.D.;
Behavioral Modeling and Simulation, 2001. BMAS 2001. Proceedings of the Fifth IEEE International Workshop on , 10-12 Oct. 2001
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Computer Design, 2001. ICCD 2001. Proceedings. 2001 International Conference on , 23-26 Sept. 2001
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